

What is claimed is:

1. A method for generating a circuit layout comprising:

selecting at least one via that has at least one edge touching an edge of an overlying metal line;

measuring a distance between the edge of the overlying metal line and an edge of an

5 adjacent metal line;

if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is at least a predetermined distance, then increasing the size of the overlying metal line; and

10 if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is less than the predetermined distance, then increasing a size of the overlying metal line and decreasing a size of the adjacent metal line.

2. The method according to claim 1, comprising increasing the size of the overlying metal line in a vicinity of the via.

3. The method according to claim 2, comprising increasing the size of the overlying metal line according to a 3 sigma via-to-metal size and positioning error factor for the technology embodied in the computer generated circuit layout.

4. The method according to claim 2, if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is less than the predetermined distance, comprising:

5 decreasing the size of the adjacent metal line by an amount that accounts for the predetermined distance and a distance delta that is determined from evaluation of simulated and experimental measurements of a distance where one metal line does not impact an adjacent metal line; and

10 increasing the size of the overlying metal line by an amount based upon evaluation of simulated and experimental measurements of a distance where one metal line does not impact an adjacent metal line

5. The method according to claim 1, further comprising:

placing the selected vias into a first group.

6. The method according to claim 5, further comprising:

placing vias from the first group that touch an overlying metal line where the distance between the overlying metal line and the edge of the adjacent metal line is at least a predetermined distance into a second group;

- 5 placing vias from the first group that are not in the second group into a third group; and
 increasing the size of overlying metal lines for metal lines touching vias in the second group.

7. The method according to claim 6, further comprising:

increasing the size of overlying metal lines and decreasing the size of adjacent metal lines for metal lines touching vias in the third group.

8. A method for generating a circuit layout comprising:

determining a minimum distance between metal lines based upon design rules that allows one metal line to be increased by a first oversize;

determining the first oversize based upon a 3 sigma via-to-metal size and positioning error factor

- 5 for the technology embodied in the circuit layout;

determining a delta distance based upon simulated and experimental measurements of metal lines in the circuit layout such that a metal line reduced by at least the delta distance will not electrically impact an adjacent metal line that is increased by a second oversize;

- determining the second oversize based upon simulated and experimental measurements of
10 metal lines in the circuit layout such that increasing a metal line by the second oversize will not electrically impact an adjacent metal line that has been decreased by at least the delta distance;

identifying a first layout layer containing vias;

identifying a second layout layer containing metal lines that contact vias that are in the first layer;

- 15 selecting vias that do not fully contact a metal line based upon whether at least one edge of a via touches an edge of an overlying metal line, and grouping the selected vias into a first via group;

- selecting vias in the first via group based upon whether a distance from the overlying metal line edge to an edge of an adjacent metal line is at least the minimum distance, and grouping these
20 selected vias into a second via group;

increasing the size of the overlying metal lines that contact vias in the second via group by the first oversize;

increasing the size of metal lines that contact vias in the first via group that are not in the second via group by the second oversize; and

25 decreasing the size of adjacent metal lines to each overlying metal line touched by a via in the first via group that is not in the second via group by at least the delta distance.

9. The method according to claim 8, wherein increasing the size of the overlying metal lines that contact vias in the second via group comprises:

increasing the size of the vias in the second via group by the first oversize;

projecting the increased size of the vias in the second via group onto the overlying metal

5 lines that contact the vias in the second via group; and

incorporating as part of the metal lines that contact the vias in the second via group the projected, increased size of the vias in the second via group.

10. The method according to claim 8, wherein increasing the size of the overlying metal lines that contact vias in the first via group that are not in the second via group comprises:

increasing the size of the vias in the first via group that are not in the second via group by the second oversize;

5 projecting the increased size of the vias in the first via group that are not in the second via group onto the overlying metal lines that contact the vias in the first via group that are not in the second via group; and

incorporating as part of the overlying metal lines that contact the vias in the first via group that are not in the second via group the projected, increased size of the vias in the first via group
10 that are not in the second via group.

11. The method according to claim 8, wherein decreasing the size of adjacent metal lines comprises:

increasing the size of the vias in the first via group that are not in the second via group by the minimum distance plus the delta distance;

5 identifying an intersection between each via increased by the minimum distance plus the delta distance and the adjacent metal lines;

projecting each intersection onto the adjacent metal lines; and

removing the projected intersection from each adjacent metal line.

12. An apparatus for generating circuit layouts comprising:

a central processing unit;

a display; and

at least an input device; wherein

5 the central processing unit:

determines a minimum distance between metal lines based upon design rules that allows one metal line to be increased by a first oversize;
 determining the first oversize based upon a 3 sigma via-to-metal size and positioning error factor for the technology embodied in the circuit layout;

- 10 determines a delta distance based upon simulated and experimental measurements of metal lines in the circuit layout such that a metal line reduced by at least the delta distance will not electrically impact an adjacent metal line that is increased by a second oversize;

determines the second oversize based upon simulated and experimental measurements of metal lines in the circuit layout such that increasing a metal line by the second oversize will not

- 15 electrically impact an adjacent metal line that has been decreased by at least the delta distance;

identifies a first layout layer containing vias;

identifies a second layout layer containing metal lines that contact vias that are in the first layer;

- 20 selects vias that do not fully contact a metal line based upon whether at least one edge of a via touches an edge of an overlying metal line, and grouping the selected vias into a first via group;

selects vias in the first via group based upon whether a distance from the overlying metal line edge to an edge of an adjacent metal line is at least the minimum distance, and grouping these selected vias into a second via group;

- 25 increases the size of the overlying metal lines that contact vias in the second via group by the first oversize;

increases the size of metal lines that contact vias in the first via group that are not in the second via group by the second oversize; and

decreases the size of adjacent metal lines to each overlying metal line touched by a via in the first via group that is not in the second via group by at least the delta distance.

13. An apparatus for generating circuit layouts comprising:

a central processing unit;

a display; and

at least an input device; wherein

- 5 the central processing unit:

selects at least one via that has at least one edge touching an edge of an overlying metal line;

measures a distance between the edge of the overlying metal line and an edge of an adjacent metal line;

10 if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is at least a predetermined distance, then increases the size of the overlying metal line; and

15 if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is less than the predetermined distance, then increases a size of the overlying metal line and decreasing a size of the adjacent metal line.

14. A computer-readable medium bearing instructions for processing a computer generated circuit layout, said instructions, when executed, are arranged to cause a computer system to perform the steps of:

5 determining a minimum distance between metal lines based upon design rules that allows one metal line to be increased by a first oversize;

determining the first oversize based upon a 3 sigma via-to-metal size and positioning error factor for the technology embodied in the circuit layout;

10 determining a delta distance based upon simulated and experimental measurements of metal lines in the circuit layout such that a metal line reduced by at least the delta distance will not electrically impact an adjacent metal line that is increased by a second oversize;

determining the second oversize based upon simulated and experimental measurements of metal lines in the circuit layout such that increasing a metal line by the second oversize will not electrically impact an adjacent metal line that has been decreased by at least the delta distance;

15 identifying a first layout layer containing vias;

identifying a second layout layer containing metal lines that contact vias that are in the first layer;

selecting vias that do not fully contact a metal line based upon whether at least one edge of a via touches an edge of an overlying metal line, and grouping the selected vias into a first via group;

20 selecting vias in the first via group based upon whether a distance from the overlying metal line edge to an edge of an adjacent metal line is at least the minimum distance, and grouping these selected vias into a second via group;

increasing the size of the overlying metal lines that contact vias in the second via group by the first oversize;

25 increasing the size of metal lines that contact vias in the first via group that are not in the second via group by the second oversize; and

decreasing the size of adjacent metal lines to each overlying metal line touched by a via in the first via group that is not in the second via group by at least the delta distance.

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15. A computer-readable medium bearing instructions for processing a computer generated circuit layout, said instructions, when executed, are arranged to cause a computer system to perform the steps of:

- 5 selecting at least one via that has at least one edge touching an edge of an overlying metal line;
- measuring a distance between the edge of the overlying metal line and an edge of an adjacent metal line;
- if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is at least a predetermined distance, then increasing the size of the overlying
- 10 metal line; and
- if the distance between the touched edge of the overlying metal line and the edge of the adjacent metal line is less than the predetermined distance, then increasing a size of the overlying metal line and decreasing a size of the adjacent metal line.

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